

A Generalized Design Framework for Neutral Point Voltage Balance of Three Phase Vienna Rectifiers

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¹Abstract—This study proposes a generalized design framework for three phase Vienna rectifiers to handle the neutral point voltage balance issue. On the basis of the design framework, it is convenient to construct various neutral point voltage balancing methods with the guarantee of stability. As demonstration, three representative neutral point voltage balance approaches are presented by choosing different zero sequence voltages. A comprehensive comparison among the three approaches are given in the aspects of input current quality, capacitor voltage fluctuation, and system efficiency. The comparison results provide a guidance for constructing the most appropriate approach based on the specific requirement. Finally, simulation and experimental results verify the correctness and effectiveness of the presented approaches and the related performance analysis.

Index Terms—Vienna converter, carrier-based PWM, neutral point voltage balance.

I. INTRODUCTION

Three phase Vienna rectifier has attracted much attention due to its advantages of low cost, low current total harmonic distortion (THD), low device voltage stress, high power density, and high efficiency [1]-[3]. Thus, it is widely used in telecommunications systems, aircraft and wind turbine systems and other areas [1], [4]-[7].

The Vienna rectifier is essentially a non-regenerative three level boost converter. In recent years, the related research mainly involves control methods and modulation strategies. There have been a lot of control schemes for the Vienna rectifier. In [1], a hysteresis current control method is proposed to regulate the input currents of Vienna rectifiers. The advantages of the hysteresis control are that it is robust and the complicated modulation strategy can be omitted. In [8], proportional-integral (PI) controllers are used based on the

average $d-q$ model of the Vienna rectifier, and a new multiple-input multiple-output linear control scheme is proposed in [9] based on the small signal model of Vienna rectifiers. To improve dynamic performance, a basic one cycle control (OCC) strategy is proposed in [10]. However, the utilization ratio of the dc-link voltage is low. Then, an improved OCC control scheme is presented, which improves the dc-link voltage utilization and efficiency [11]. To reduce the costs, a voltage sensor-less control is introduced for the Vienna rectifier [12], in which the grid voltage is estimated by an observer. On the other hand, a current sensor-less control scheme is presented in [13]. Besides, a direct power control scheme based on sliding mode control is proposed to improve the dynamic response and robustness [14]. In the cases of unbalanced power supplies, a control scheme based on positive and negative sequence decomposition is introduced, which eliminates the dc-link voltage ripples [15]-[16].

Additionally, various modulation methods have been proposed for Vienna rectifiers. They can mainly be divided into two categories: space vector modulation (SVM) and carrier-based pulse width modulation (PWM) methods. In [17]-[18], the basic SVM approaches for the three phase Vienna rectifier are investigated, and a discontinuous SVM method is proposed in [19] to reduce power losses. According to [20], there always exists a carrier-based PWM that is equivalent to its corresponding SVM in three phase voltage source inverters. The equivalence of SVM and carrier-based PWM is studied in detail for the Vienna rectifier [21]. On the basis of the equivalence, a carrier-based PWM algorithm is proposed in [22]. To enhance efficiency and accommodate variable power factor operation, a discontinuous carrier-based PWM method is presented [23]-[24].

Due to the characteristics of three-level power converters, neutral point voltage balance control is very essential in Vienna rectifiers. Unbalanced neutral point voltages will change the voltage stress on the switching devices and degrade the system performance. In SVM, the neutral point voltage balance is usually realized by adjusting the dwell time of the redundant short vectors [21]-[22], [25]. The dwell time ratio of the redundant vectors is determined by a PI or proportional controller. However, the design and stability of the neutral point voltage balance controller is not introduced in detail. On the other hand, the neutral point voltage balance is realized by regulating the zero sequence signals [21]-[22] in carrier based-PWM schemes. The principle to maintain the neutral point voltage balance in the framework of carrier based-PWM is discussed intensively [8]. And the method could effectively

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eliminate neutral point voltage fluctuation. Based on the same principle, a hybrid control is proposed to suppress the third-harmonic component in the neutral point voltage [26]. On the basis of the equivalence of SVM and carrier-based PWM, a carrier-based PWM method with neutral point voltage balance is presented in [22]. A discontinuous carrier-based PWM with neutral point voltage balance is proposed and the performance evaluation is carried out in [23], [27]. Besides, there are some other neutral point voltage balance methods. For instance, in the hysteresis control [1], [28], a zero sequence current generated by a PI controller is added to the input current reference for neutral point voltage balance. Recently, a finite set model predictive control for Vienna rectifiers is presented in [29]. The neutral point voltage balance is realized by imposing the capacitor voltage error into the cost functions.

Though many neutral point voltage balance methods have been proposed, most of them lack the systematic design and in-depth stability analysis. In this study, a generalized design framework is presented to maintain neutral point voltage balance for Vienna rectifiers. The other contributions of this study include: 1) based on the design framework, various neutral point voltage balancing methods can be constructed conveniently; 2) as demonstration, three representative neutral point balance approaches are presented under the proposed design framework; 3) the performance of the three approaches are analyzed and compared in terms of input current quality, capacitor voltage fluctuation and operating efficiency; 4) the stability of the three approaches have been proven, and it is found that approach I is stable in the common sense, approach II and III are stable in the average sense, while the stability of approach III belongs to input-to-state stability; 5) neutral point voltage self-balancing can be achieved without adding extra feedback control actions under the proposed approaches.

The remainder of this paper is organized as follows. Section II presents the system model of the three-phase Vienna rectifier. Then, the carrier-based PWM strategy is described in Section III. In Section IV, the proposed design framework for neutral point voltage balance is introduced in detail, as well as the three approaches derived from the framework. In Section V, the performance analysis among these approaches is described. In Section VI, the simulation and experimental results are presented and discussed, and finally, the main points of this paper are summarized in Section VII.

II. MODELING OF THREE-PHASE VIENNA RECTIFIER

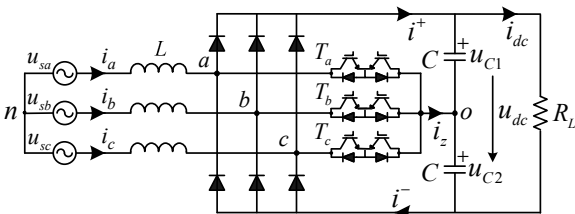


Fig. 1 Circuit topology of the three-phase Vienna rectifier.

Fig. 1 shows the circuit configuration of three-phase Vienna rectifier, which is composed of a three-phase diode bridge and three bidirectional switches connecting the input phases to the dc-link neutral point. Besides, two split capacitors are located at

the dc-link. According to Fig. 1, an equivalent circuit of the three-phase Vienna rectifier is shown in Fig. 2.

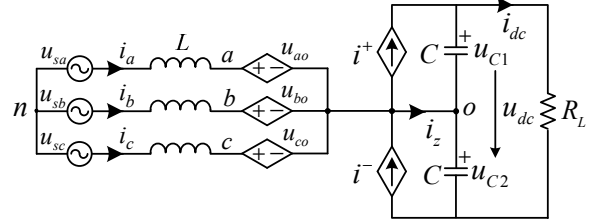


Fig. 2 Equivalent circuit of the three-phase Vienna rectifier.

Denote S_x as the switching state of the bidirectional switch T_x in Fig. 1, and $x \in \{a, b, c\}$. $S_x = 1$ means the switch is on; $S_x = 0$ means the switch is off.

The input current dynamics are given as

$$\begin{cases} L \frac{di_a}{dt} = u_{sa} - u_{an} \\ L \frac{di_b}{dt} = u_{sb} - u_{bn} \\ L \frac{di_c}{dt} = u_{sc} - u_{cn} \end{cases} \quad (1)$$

where L is the filter inductance. u_{sx} and i_x are the source voltages and phase currents, respectively. u_{xn} are the input voltages (referred to the ac neutral point n), which could be

$$\begin{cases} u_{an} = u_{ao} - u_{no} \\ u_{bn} = u_{bo} - u_{no} \\ u_{cn} = u_{co} - u_{no} \end{cases} \quad (2)$$

In (2), u_{no} is the zero sequence voltage, and u_{xo} are semi-controllable voltages (referred to the dc-link neutral point o). Due to the structural characteristics of the Vienna rectifier, u_{xo} is determined not only by the status of the bidirectional switch, but also by the input current direction. Thus, it is called the semi-controllable voltage. For convenience, u_{xo} could be expressed precisely in such a compact way as:

$$\begin{cases} u_{ao} = (1 - S_a)H_a = (1 - S_a) \left[\frac{\text{sgn}(i_a)+1}{2}u_{C1} + \frac{\text{sgn}(i_a)-1}{2}u_{C2} \right] \\ u_{bo} = (1 - S_b)H_b = (1 - S_b) \left[\frac{\text{sgn}(i_b)+1}{2}u_{C1} + \frac{\text{sgn}(i_b)-1}{2}u_{C2} \right] \\ u_{co} = (1 - S_c)H_c = (1 - S_c) \left[\frac{\text{sgn}(i_c)+1}{2}u_{C1} + \frac{\text{sgn}(i_c)-1}{2}u_{C2} \right] \end{cases} \quad (3)$$

where $\text{sgn}()$ is the sign function that is used to distinguish the input current directions. u_{C1} and u_{C2} represent the related voltages across the upper and lower capacitors, respectively. Note that u_{xo} in (3) refers to the actual capacitor voltages, rather than the assumed capacitor voltages that equal to the half of the dc-link voltage.

The dynamic equations of the two capacitors can be given as

$$\begin{cases} C \frac{du_{C1}}{dt} = i^+ - i_{dc} \\ C \frac{du_{C2}}{dt} = i^- - i_{dc} \end{cases} \quad (4)$$

where C represents the capacitance of the two capacitors, and i_{dc} is the load current. i^+ and i^- are the currents through the positive and negative dc-bus, which can be formulated as

$$\begin{cases} i^+ = \sum_{x=a,b,c} \left\{ (1-S_x) \left[\frac{\text{sgn}(i_x)+1}{2} \right] i_x \right\} \\ i^- = \sum_{x=a,b,c} \left\{ (1-S_x) \left[\frac{\text{sgn}(i_x)-1}{2} \right] i_x \right\} \end{cases} \quad (5)$$

III. CARRIER-BASED MODULATION STRATEGY FOR THE VIENNA RECTIFIER

Assume that the source voltages and input currents are balanced and sinusoidal. Then, u_{xn} and i_x in the steady state could be expressed as

$$\begin{cases} u_{an} = U_m \sin(\omega t) \\ u_{bn} = U_m \sin(\omega t - \frac{2\pi}{3}) \\ u_{cn} = U_m \sin(\omega t + \frac{2\pi}{3}) \end{cases} \quad (6)$$

$$\begin{cases} i_a = I_m \sin(\omega t + \varphi_i) \\ i_b = I_m \sin(\omega t - \frac{2\pi}{3} + \varphi_i) \\ i_c = I_m \sin(\omega t + \frac{2\pi}{3} + \varphi_i) \end{cases} \quad (7)$$

where ω is the input angular frequency; I_m is the magnitude of i_x ; φ_i is the displacement angle between u_{xn} and i_x , which is different from the input power factor angle φ_s due to the input filtering inductor L . U_m is the magnitude of u_{xn} , which can be determined by the known i_x and L .

Take the average of both sides of (3) over a switching period, and then combine (2), the duty cycles d_x of the bidirectional switches can be given directly as

$$\begin{cases} d_a = 1 - \frac{u_{an} + u_{no}}{H_a} \\ d_b = 1 - \frac{u_{bn} + u_{no}}{H_b} \\ d_c = 1 - \frac{u_{cn} + u_{no}}{H_c} \end{cases} \quad (8)$$

With the H_x in (3), the duty cycle calculations in (8) will use the actual capacitor voltages.

In carrier-based PWM methods, it is essential to choose a proper zero sequence voltage u_{no} for enhancing dc-link voltage utilization. First, the feasible range of u_{no} could be determined.

According to (2), the following inequalities can be obtained.

$$\begin{cases} u_{ao,\min} - u_{an} \leq u_{no} = u_{ao} - u_{an} \leq u_{ao,\max} - u_{an} \\ u_{bo,\min} - u_{bn} \leq u_{no} = u_{bo} - u_{bn} \leq u_{bo,\max} - u_{bn} \\ u_{co,\min} - u_{cn} \leq u_{no} = u_{co} - u_{cn} \leq u_{co,\max} - u_{cn} \end{cases} \quad (9)$$

where

$$\begin{cases} u_{xo,\max} = \frac{\text{sgn}(i_x)+1}{2} u_{C1} \\ u_{xo,\min} = \frac{\text{sgn}(i_x)-1}{2} u_{C2} \end{cases} \text{ and } x \in \{a, b, c\}.$$

Then, the feasible range of u_{no} is expressed as follows.

$$u_{no} \in [u_{no,\min}, u_{no,\max}] \quad (10)$$

where

$$\begin{aligned} u_{no,\min} &= -\frac{u_{C2}}{2} + \max \left(\frac{\text{sgn}(i_a)u_{C2}}{2} - u_{an}, \frac{\text{sgn}(i_b)u_{C2}}{2} - u_{bn}, \frac{\text{sgn}(i_c)u_{C2}}{2} - u_{cn} \right), \\ u_{no,\max} &= \frac{u_{C1}}{2} + \min \left(\frac{\text{sgn}(i_a)u_{C1}}{2} - u_{an}, \frac{\text{sgn}(i_b)u_{C1}}{2} - u_{bn}, \frac{\text{sgn}(i_c)u_{C1}}{2} - u_{cn} \right). \end{aligned}$$

Clearly, the feasible range of u_{no} is related to the input current directions and capacitor voltages, which are time-varying. However, if $u_{no,\min} \leq u_{no,\max}$, there will always exist a zero-sequence voltage that makes the modulation strategy feasible.

IV. PROPOSED DESIGN FRAMEWORK FOR NEUTRAL POINT VOLTAGE BALANCE

Combine (4) and (5), and then consider the switching period average method, it leads to

$$C \frac{d\tilde{u}}{dt} = i^+ - i^- = -d_a i_a - d_b i_b - d_c i_c \quad (11)$$

where $\tilde{u}$ is the error between capacitor voltages u_{C1} and u_{C2} .

After substituting (6)-(8) into (11), and performing some simplifications, (11) can then be formulated as

$$\frac{d\tilde{u}}{dt} = \alpha f(t, \tilde{u}) = \alpha [(J + Nu_{no}) - K\tilde{u}] \quad (12)$$

where

$$\begin{aligned} \alpha &= \frac{2}{C(u_{dc}^2 - \tilde{u}^2)}; \\ J &= u_{dc} \sum_{x=a,b,c} (u_{xn} |i_x|); \\ N &= u_{dc} \sum_{x=a,b,c} |i_x|; \\ K &= \sum_{x=a,b,c} (u_{xn} i_x). \end{aligned}$$

In (12), u_{dc} is the dc-link voltage. Usually, $u_{dc} > 0$, thus $N > 0$. K can be rewritten as $K = \frac{3}{2} U_m I_m \cos(\varphi_i)$. Since φ_i is confined within $[-\frac{\pi}{6}, \frac{\pi}{6}]$, K is always a positive constant. If $\tilde{u}$ is small relative to u_{dc} , then $\alpha \approx \frac{2}{Cu_{dc}^2} > 0$.

According to (12), the selection of u_{no} is critical to determine whether $\tilde{u}$ can converge to zero, leading to neutral point voltage balance. In this study, a generalized design framework for neutral point voltage balance will be introduced, which mainly involves the selection of u_{no} .

Let u_{no} be divided into two parts, expressed as

$$u_{no} = u'_{no} + u''_{no} \quad (13)$$

In (13), u'_{no} represents a feed-forward term, and $u''_{no} (= k\tilde{u})$ is a feedback term, where k is an adjustable coefficient. Note that, if $k = 0$, the feedback term will be null.

Substituting (13) into (12), it yields

$$\frac{d\tilde{u}}{dt} = \alpha f(t, \tilde{u}) = \alpha \left[(J + Nu'_{no}) + (\bar{N}k - K)\tilde{u} \right] \quad (14)$$

To verify the convergence of (14), the average theory [30] is considered. According to the averaging theory, let $f(t, x)$ and its partial derivatives be continuous and bounded for $(t, x) \in [t_0, \infty) \times D$, then, for the system $\dot{x} = \varepsilon f(t, x)$ (ε is a small positive value, and $f(t, x)$ is T -periodic in t), the solution $x(t)$ can be approximated by the solution of an "averaged system" $\dot{x} = \varepsilon f_{av}(x)$, where

$$f_{av}(x) = \frac{1}{T} \int_0^T f(t, x) dt \quad (15)$$

Assume that u_{dc} has been well regulated by a dc voltage controller. By numerical calculations, it is easy to verify that both J and N in (14) are T_i -periodic functions in t , where $T_i (= \frac{2\pi}{\omega})$ is the power source period. Thus, with a proper selection of u'_{no} , the $f(t, \tilde{u})$ in (14) can be seen as a T_i -periodic function.

As the positive parameter α is relatively small, the averaging theory could be applied to (14). Then, the related "averaged system" can be derived as

$$\frac{d\bar{\tilde{u}}}{dt} = \alpha \left[\frac{1}{T_i} \int_0^{T_i} (J + Nu'_{no}) dt + (\bar{N}k - K)\bar{\tilde{u}} \right] \quad (16)$$

where $\bar{\tilde{u}}$ is the averaged voltage error and represents the solution of the "averaged system", and $\bar{N}$ is the average value of N , as formulated in (17).

$$\bar{N} = \frac{1}{T_i} \int_0^{T_i} N dt = \frac{6I_m u_{dc}}{\pi} \quad (17)$$

Observe (16), to guarantee the asymptotic stability, u'_{no} and k should meet the following conditions.

$$\begin{cases} \frac{1}{T_i} \int_0^{T_i} (J + Nu'_{no}) dt = 0 \\ \bar{N}k - K < 0 \end{cases} \quad (18)$$

Moreover, based on the carrier-based modulation principle, u_{no} should be within the range $[u_{no,min}, u_{no,max}]$. However, if the dc capacitances are large enough, the feedback term u'_{no} will be negligible or even be zero in the steady state. Then, it is practical to just ensure the feed-forward term u'_{no} stays in the range.

As a result, a generalized design framework for neutral voltage point balance can be summarized as follows:

$$\begin{cases} \frac{1}{T_i} \int_0^{T_i} (J + Nu'_{no}) dt = 0 \\ u_{no,min} \leq u'_{no} \leq u_{no,max} \\ \bar{N}k - K < 0 \end{cases} \quad (19)$$

With the proposed design framework, it is convenient to construct various neutral point voltage balance methods. Also, it by selecting proper u'_{no} and k . Such design framework combines the control system stability and carrier-based modulation principle, so both the dynamic and steady state performance are taken into account. It is worth noting that the selections of u'_{no} and k have different functions. More specifically, the coefficient k that is contained in the feedback term u'_{no} mainly determines the convergence rate of voltage error dynamic; while the feed-forward term u'_{no} concerns the steady-state operating performance.

With a qualified u'_{no} , k should just meet $\bar{N}k - K < 0$. In particular, if $k = 0$, (16) can be simplified to

$$\frac{d\bar{\tilde{u}}}{dt} = -\alpha K \bar{\tilde{u}} \quad (20)$$

As seen, (20) is asymptotically stable, and the convergence rate of $\bar{\tilde{u}}$ is determined by αK , which is related to the system parameters and can barely be adjusted. In other words, the neutral point voltage can be self-balanced despite the lack of feedback control actions. However, to speed up the convergence rate or enhance the neutral point voltage balance capability, a proper k of less than zero will be more suitable. So far, only the ideal case is considered where there are no non-symmetric dc output currents in the Vienna rectifier. In the presence of permanent non-symmetric dc output currents, the feedback term u'_{no} in (13) should be revised as $u'_{no} = k_p \tilde{u} + k_i \int \tilde{u} dt$ to maintain neutral point voltage balance, which is the output of a PI controller. To ensure the stability, both k_p and k_i are less than zero.

With a proper k , the selection of u'_{no} should be paid more attention. Because it embodies the most essential feature of neutral point voltage balancing methods. In the following subsections, three approaches to selecting u'_{no} will be presented from different aspects.

A. Approach I

In approach I, let $J + Nu'_{no} = 0$, then, $u'_{no,I}$ is

$$u'_{no,I} = -\frac{J}{N} = -\frac{\sum_{x=a,b,c} (u_{xn} |i_x|)}{\sum_{x=a,b,c} |i_x|} \quad (21)$$

In this case, the original voltage error dynamic (14) can be considered rather than the averaged system (16). Substituting (21) into (14), it leads to

$$\frac{d\tilde{u}}{dt} = -\alpha (K - Nk) \tilde{u} \quad (22)$$

where the actual voltage error $\tilde{u}$ can directly converge to zero, with a proper k .

From the viewpoint of modulation, $u'_{no,I}$ should be within $[u_{no,min}, u_{no,max}]$ to ensure the valid carrier-based PWM. By

analysis, $u'_{no,I}$ can strictly satisfy $u_{no,min} \leq u'_{no,I} \leq u_{no,max}$ only at $\varphi_i = 0$; while in other conditions, $u'_{no,I}$ will be outside the range at certain time points. Such feature may affect input current quality, which will be discussed in the next section.

Note that, this approach is similar to the feed-forward quantity of the control scheme in [8]. However, it assumed $u_{C1} = u_{C2}$ in [8] when modeling the system, and feedback control must be used.

B. Approach II

In approach II, u'_{no} can take the intermediate value of the range (10), which is

$$u'_{no} = \frac{1}{2}(u_{no,min} + u_{no,max}) \quad (23)$$

where the u'_{no} in (23) will be always within its feasible range.

However, u'_{no} in (23) will fail to ensure the neutral point voltage balance, when a large deviation occurs between the two capacitor voltages at $k = 0$. Then, a modified selection for u'_{no} is designed in approach II based on (23), as expressed in (24).

$$u'_{no,II} = \frac{1}{2}(u_{no,min}^c + u_{no,max}^c) \quad (24)$$

where

$$u_{no,min}^c = -\frac{u_C}{2} + \max\left(\frac{\text{sgn}(i_a)u_C}{2} - u_{an}, \frac{\text{sgn}(i_b)u_C}{2} - u_{bn}, \frac{\text{sgn}(i_c)u_C}{2} - u_{cn}\right),$$

$$u_{no,max}^c = \frac{u_C}{2} + \min\left(\frac{\text{sgn}(i_a)u_C}{2} - u_{an}, \frac{\text{sgn}(i_b)u_C}{2} - u_{bn}, \frac{\text{sgn}(i_c)u_C}{2} - u_{cn}\right),$$

$$u_C = \frac{1}{2}(u_{C1} + u_{C2}).$$

Compare (23) with (24), the difference lies in that a fictitious u_C in (24) is used to replace u_{C1} and u_{C2} , and it equals to the average of the two. When the capacitor voltages are balanced, there will be little difference between (23) and (24).

By numerical calculations, it can be verified that $u'_{no,II}$ is T_i -periodic, and

$$\frac{1}{T_i} \int_0^{T_i} (J + Nu'_{no,II}) dt = 0 \quad (25)$$

Substituting (25) into the averaged system (16), it leads to

$$\frac{d\bar{u}}{dt} = -\alpha(K - \bar{N}k)\bar{u} \quad (26)$$

As seen, the averaged form of (26) is very similar to (22). Here, the neutral point voltage balance in the average sense can be guaranteed with $u'_{no,II}$.

C. Approach III

In addition to the continuous modulation, discontinuous carrier-based PWM strategy has the advantage of reducing switching loss, which can also be used in the three-phase Vienna rectifier.

In approach III, u'_{no} is designed by choosing its boundary values of the range, which is

$$u'_{no,III} = \begin{cases} u_{no,min}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \\ u_{no,max}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \end{cases} \quad (27)$$

where $u_{no,min}^c$ and $u_{no,max}^c$ are the same as in (24). In addition to (27), u'_{no} can also be designed in other forms of discontinuous PWM, such as in (28).

$$u'_{no,III} = \begin{cases} u_{no,max}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \\ u_{no,min}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \end{cases} \quad (28)$$

After some manipulations with (27) or (28), it can be verified that the average values of $J + Nu'_{no,III}$ are zero. Consider the averaging theory, the averaged system in approach III is the same as (26), by which the related stability can be verified with $u'_{no,III}$.

However, by using (27) or (28), one of the bidirectional switches can retain on or off-state for one modulation period, only if the two capacitor voltages are strictly identical in the steady state. However, the averaging theory-based stability criteria can only ensure that the two capacitor voltages have the same average values, rather than the actual values. Thus, it is difficult to keep one of the switches being on or off for the entire switching period. In that case, the discontinuous carrier-based PWM cannot be fully accomplished.

Therefore, in actual implementation process, $u'_{no,III}$ in (27) and (28) will be revised to (29) and (30), respectively.

$$u'_{no,III} = \begin{cases} u_{no,min}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \text{ and } |u_{no,min}^c - u_{no,min}| > \beta \\ u_{no,min}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \text{ and } |u_{no,min}^c - u_{no,min}| \leq \beta \\ u_{no,max}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \text{ and } |u_{no,max}^c - u_{no,max}| > \beta \\ u_{no,max}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \text{ and } |u_{no,max}^c - u_{no,max}| \leq \beta \end{cases} \quad (29)$$

$$u'_{no,III} = \begin{cases} u_{no,max}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \text{ and } |u_{no,min}^c - u_{no,min}| > \beta \\ u_{no,max}^c, & \text{if } |u_{no,min}^c| \geq |u_{no,max}^c| \text{ and } |u_{no,min}^c - u_{no,min}| \leq \beta \\ u_{no,min}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \text{ and } |u_{no,max}^c - u_{no,max}| > \beta \\ u_{no,min}^c, & \text{if } |u_{no,min}^c| < |u_{no,max}^c| \text{ and } |u_{no,max}^c - u_{no,max}| \leq \beta \end{cases} \quad (30)$$

where β is a small positive value, and is related to the capacitor voltage difference in the steady state.

By comparisons, it is clear that $u'_{no,III} = u'_{no,III} + \Delta$, and $|\Delta| \leq \beta$. Since the average values of $J + Nu'_{no,III}$ are zero, it can lead to

$$\begin{aligned} \frac{d\bar{u}}{dt} &= -\alpha(K - \bar{N}k)\bar{u} + \frac{1}{T_i} \int_0^{T_i} \Delta dt \\ &\leq -\alpha(K - \bar{N}k)\bar{u} + \beta \end{aligned} \quad (31)$$

As β is relatively small, the "averaged system" (31) could still prove to be bounded stable. Then, the approximate neutral point voltage balance can also be guaranteed.

By using $u'_{no,III}$, when the averaged system enters steady state, the actual boundary values of u'_{no} will be used. Therefore, the actual discontinuous PWM can be realized, which is favorable to improve the operating efficiency.

From approach III, it is found that the selection of u'_{no} in the proposed design framework can be further relaxed to: $\left| \frac{1}{T_i} \int_0^{T_i} (J + Nu_{no}) dt \right| \leq \beta$, where β is a small positive value.

In summary, from the viewpoint of stability, approach I can stay stable in the common sense; approach II and III are stable in the average sense; while the stability of approach III belongs to input-to-state stability.

In addition to the above approaches, there are still other ways to construct u'_{no} . If the constructed method satisfies the generalized design framework above, it must be effective to maintain neutral point voltage balance.

V. PERFORMANCE ANALYSIS FOR THE APPROACHES

For the above three approaches, the related steady-state performance will be discussed in this section.

A. Neutral Point Voltage Balance Performance

In approach I, the capacitor voltage error is governed by the original dynamic system (22). Clearly, the actual voltage error will converge to zero as time tends to infinity. In other words, the two capacitor voltages can coincide well with each other.

Unlike approach I, both approach II and III deal with the averaged voltage error, relying on the "averaged system" (26). Though the average voltage errors converge to zero, they cannot give all the information of the actual capacitor voltages. Furthermore, the actual capacitor voltage errors in approach II and III are different.

To evaluate the neutral point voltage balance performance, the standard deviations of capacitor voltage error are calculated for the three approaches. Consider (12), the following formulation in (32) can be used to approximate the standard deviation.

$$\sigma = \frac{1}{u_{dc}^2} \sqrt{\frac{1}{T_i} \int_0^{T_i} (J + Nu'_{no})^2 dt} \quad (32)$$

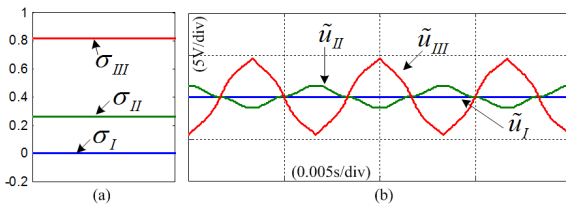


Fig. 3 diagrams in approach I,II and III: (a) the approximated standard deviation of $\tilde{u}$; (b) the waveforms of $\tilde{u}$.

The results in Fig. 3(a) indicate that $\sigma_{III} > \sigma_{II} > \sigma_I = 0$. Accordingly, the capacitor voltage errors show different variation ranges in the steady state, as shown in Fig. 3(b). To avoid repetitive works, only the first form (27) of approach III

is considered here and in the following sections. It can be inferred that, approach I will obtain the best neutral point voltage balance performance, and approach III is the worst one.

B. Input Current Quality

Beside the neutral point voltage balance performance, input current quality is also an important index to evaluate the three approaches. In such aspect, it is better for u'_{no} lying in the feasible range. From (10), it can be inferred that the feasible range of u'_{no} is actually related with input power factor.

In order to test if the selected u'_{no} in the three approaches satisfy $u_{no,min} \leq u'_{no} \leq u_{no,max}$, some numerical analysis are given in this subsection. At unity input power factor, Fig. 4 shows the corresponding steady-state waveforms of u'_{no} , $u_{no,min}$, $u_{no,max}$ in approach I, II, and III, respectively. Note that all the voltage quantities are normalized by the dc-link voltage. As seen, the inequality $u_{no,min} \leq u_{no,max}$ holds. Moreover, both $u'_{no,II}$ and $u'_{no,III}$ lie in the feasible range at any time. However, $u'_{no,I}$ is within $[u_{no,min}, u_{no,max}]$ only in most of time, and some points of $u'_{no,I}$ are outside the feasible range.

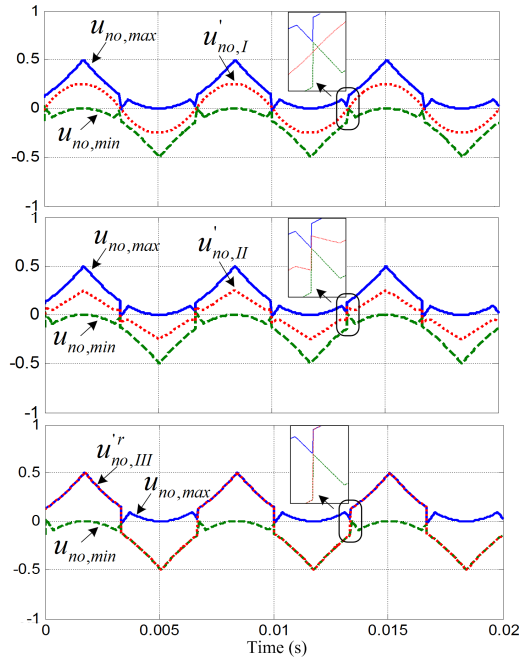


Fig. 4 Waveforms of $u_{no,min}$, $u_{no,max}$, u'_{no} in the three approaches at unity input power factor ($\phi_s = 0$).

At lower input power factor, Fig. 5 shows the related waveforms in the three approaches. As seen, $u'_{no,II}$, $u'_{no,III}$ are still within the feasible range at any time; while more points of $u'_{no,I}$ are outside the range.

In fact, $u'_{no,I}$ can completely be within the range only at $\phi_i = 0$, which means that the operating range of approach I is relatively narrow. That is the shortcoming of approach I. Because of this, approach I is prone to the input current

distortion especially at lower power factor, which is, however, not too obvious at unity input power factor. In addition, both approach I and II belong to continuous PWM; while approach III uses the discontinuous PWM. According to [31], the current quality in discontinuous PWM is usually worse than that in continuous PWM even in linear modulation region.

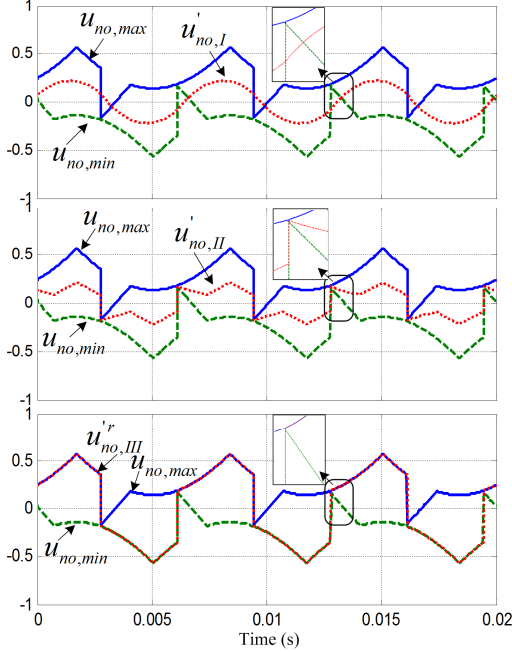


Fig. 5 Waveforms of $u_{no,min}$, $u_{no,max}$, u'_{no} in the three approaches at lower input power factor ($\phi_s = \frac{\pi}{18}$).

Based on the above analysis, approach II will have the best input current quality of the three approaches. Further, the input current quality of approach III may be worse than the other two approaches at unity input power factor. But with the decrease of input power factor, the input current distortions of approach I will be more serious than that of approach III.

VI. SIMULATION AND EXPERIMENT RESULTS

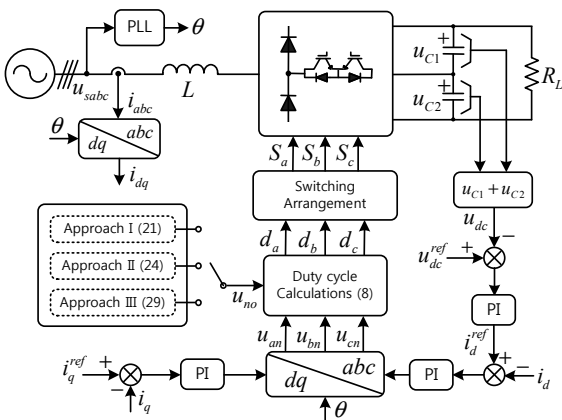


Fig. 6. Control block diagram for three phase Vienna rectifier.

To validate the proposed design framework and related performance analysis, some simulations and experiments have been carried out. Fig. 6 shows the control block diagram for the three-phase Vienna rectifier, where the dc-link voltage and input currents are regulated by PI controllers. The three

approaches differ from the selections of zero sequence voltage that will be added in the duty cycle calculations. TABLE.I lists the parameters involved in the simulations and experiments.

Symbol	Description	value
u_{il}	Input line voltage	220V(rms)
ω_l	Input angular frequency	314 rad/s
L	Input filtering inductance	3mH
C	DC-link capacitance	560μF
R_L	Load resistance	80 Ω
T_s	Modulation period	50μs

A. Simulations Results

In this subsection, some numerical simulations have been carried out in the MATLAB/Simulink platform.

To test the neutral point voltage balance capability, an unbalanced situation is constructed by connecting a resistor of 80 Ω in parallel with the upper capacitor during the time interval [0.3s, 0.31s]. The Vienna rectifier works with unity input power factor, and the desired dc-link voltage is set to 360V. Figs. 7(a)-(c) show the capacitor voltage waveforms, when the three approaches to selecting u'_{no} are used with $k = 0$.

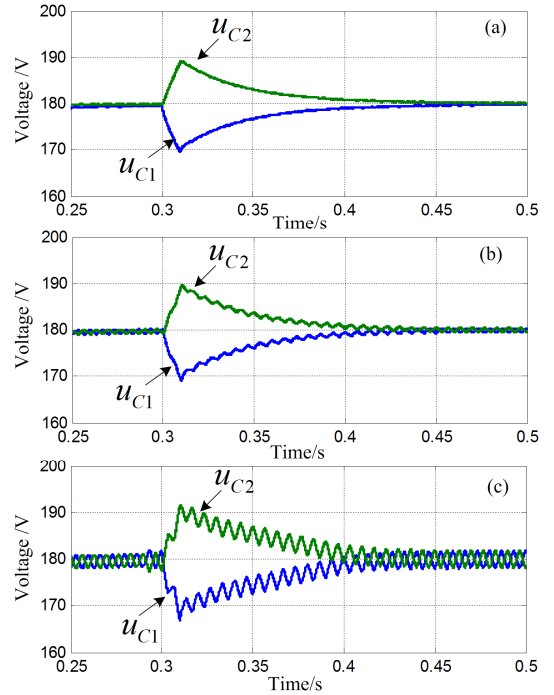


Fig. 7 Simulation results with $k = 0$ and in (a) approach I; (b) approach II; (c) approach III.

As seen, all the capacitor voltages can return to balance point gradually. Moreover, the balancing rates of capacitor voltages are almost the same, because they are all determined by αK . Besides, it is noteworthy that the capacitor voltage waveforms are different in the three approaches. The capacitor voltages in approach I are relatively smooth; while they are pulsating with different degrees in approach II and III. It is clear that the pulsation in approach III is more serious than that in

approach II. These results agree well with the related performance analysis mentioned before.

Figs. 8(a)-(c) show the capacitor voltage waveforms in approach I, II and III, when the feedback term u_{no}^* is added and $k = -3$. As seen, the voltage deviations are smaller than those in Fig. 7, and the unbalanced capacitor voltages turn into balance more rapidly. Clearly, the feedback term will help to improve neutral point voltage balance capability. Besides, the capacitor voltage waveforms also exhibit different characteristics in the three approaches, similar to the results in Fig. 7.

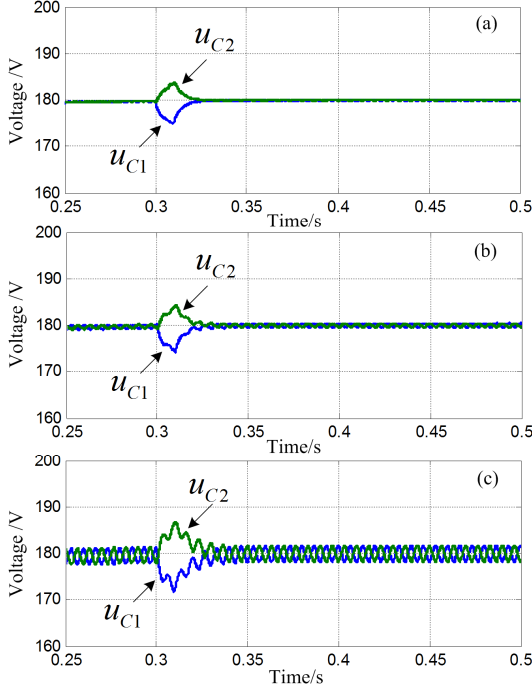


Fig. 8 Simulation results with $k = -3$ and in (a) approach I; (b) approach II; (c) approach III.

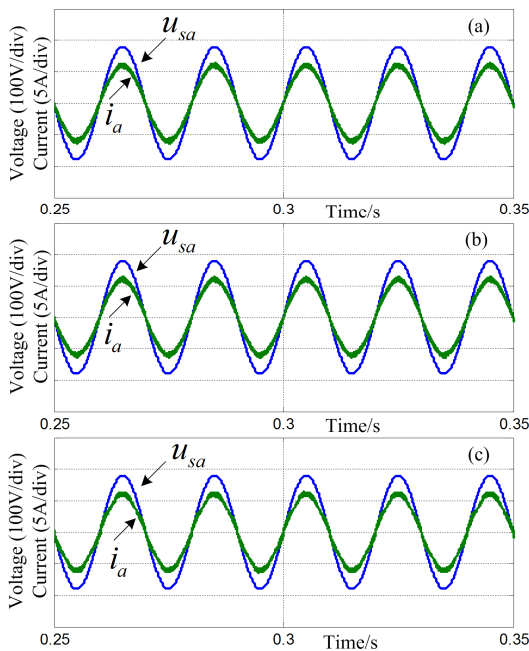


Fig. 9 Input voltage and current waveforms at unity input power factor in (a) approach I; (b) approach II; (c) approach III.

To validate the analysis about input current quality, two situations with different input power factors are tested.

Figs. 9(a)-(c) show a -phase source voltage and input current waveforms of the three approaches with unity input power factor. As seen, all the input currents are well controlled. The THDs of input currents are 3.98%, 3.84% and 4.92% in approach I, II, and III, respectively.

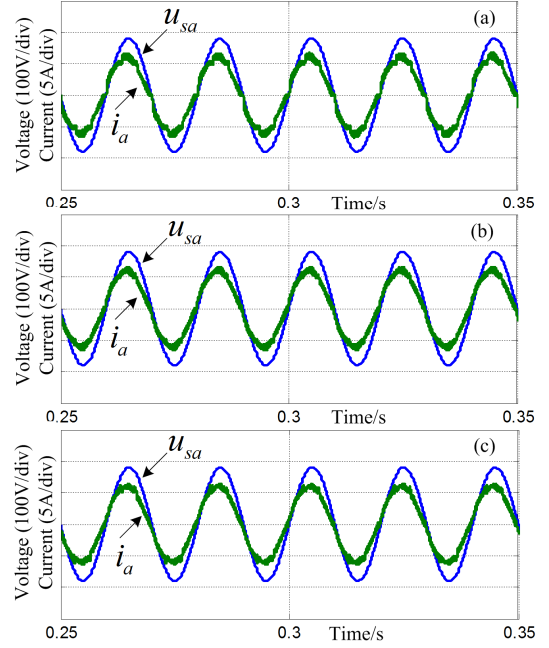


Fig. 10 Input voltage and current waveforms at $\phi_s = \frac{\pi}{18}$ in (a) approach I; (b) approach II; (c) approach III.

Figs. 10 (a)-(c) show the corresponding waveforms of the three approaches with the input power factor angle $\phi_s = \frac{\pi}{18}$. As seen, all the input currents lead the related input voltages. However, the current waveforms are a little different in these approaches. By comparisons, approach II can acquire the best input current quality ($THD_i=4.21\%$), approach III comes next ($THD_i=6.18\%$), then followed by approach I ($THD_i=8.32\%$).

Clearly, the simulation results in Fig. 9 and Fig. 10 are in good agreement with the analysis in Section IV.

B. Experimental Results

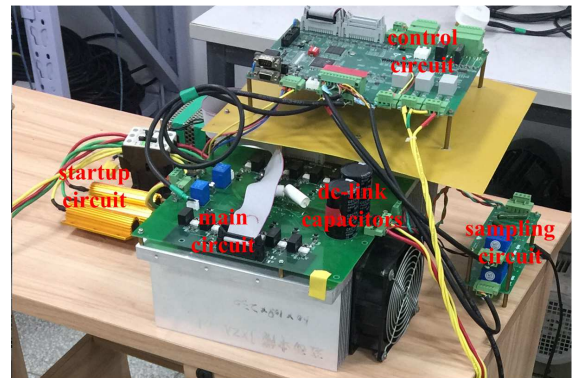


Fig. 11 Prototype of the three-phase Vienna rectifier.

A prototype of three-phase Vienna rectifier with the specifications given in TABLE. I has been built in the laboratory, as shown in Fig.11. The bidirectional switches are made up of two insulated gate bipolar transistors (IGBTs) IKW30N65EL5 (650V/30A, Infineon) with common emitter. The three phase diode bridge circuit employs six fast recovery diodes IDW40E65D1 (650V/40A, Infineon). Besides, the control platform is based on a floating-point digital signal processor (DSP) TMS320F28335.

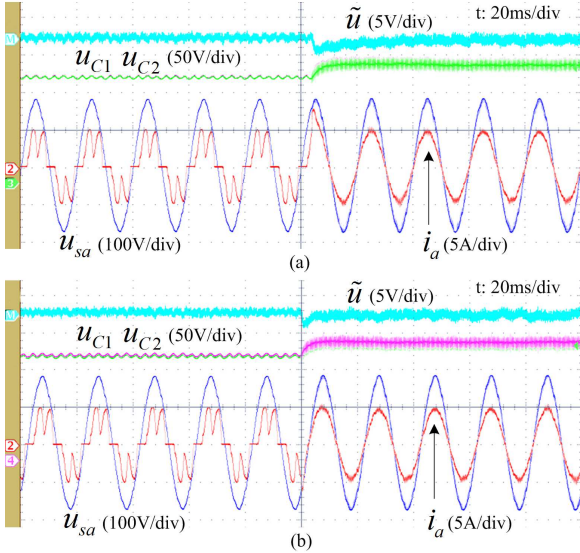


Fig. 12 Experimental results of approach I when the control system starts up in: (a) case of $k = 0$; (b) case of $k = -3$.

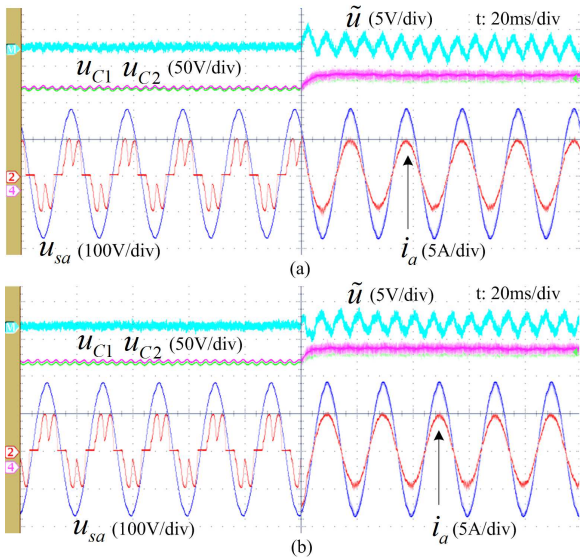


Fig. 13 Experimental results of approach II when the control system starts up in: (a) case of $k = 0$; (b) case of $k = -3$.

First, consider unity input power factor and the desired dc-link voltage is set to 320V. Fig. 12(a) shows the experimental results of approach I with $k = 0$ before and after the control system starts up, which contain the waveforms of a -phase source voltage and input current, two capacitor voltages, and the voltage error between them. Fig. 12(b) shows the experimental results of approach I with $k = -3$.

As seen, after the control system starts up, both the input

currents turn into sinusoidal quickly, and the capacitor voltages become half of the desired dc-link voltages. The input currents are in phase with the input voltages, which means that unity input power factor has been obtained. Besides, it can be inferred from the voltage error waveforms that the control system with the case of $k = -3$ has faster convergence speed than that with $k = 0$, which agrees well with the theoretic analysis.

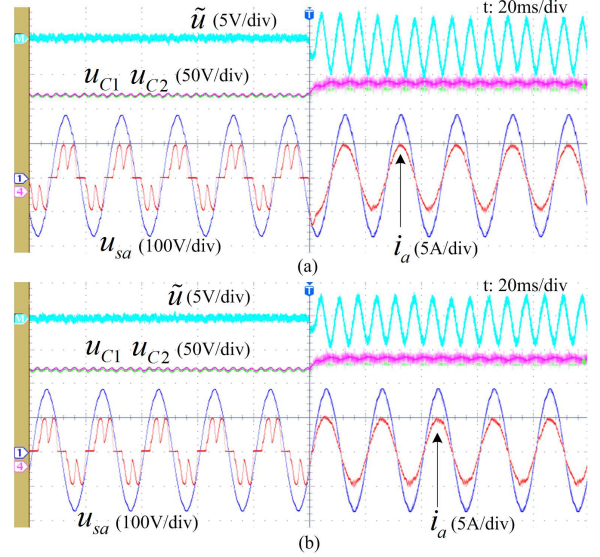


Fig. 14 Experimental results of approach III when the control system starts up in: (a) case of $k = 0$; (b) case of $k = -3$.

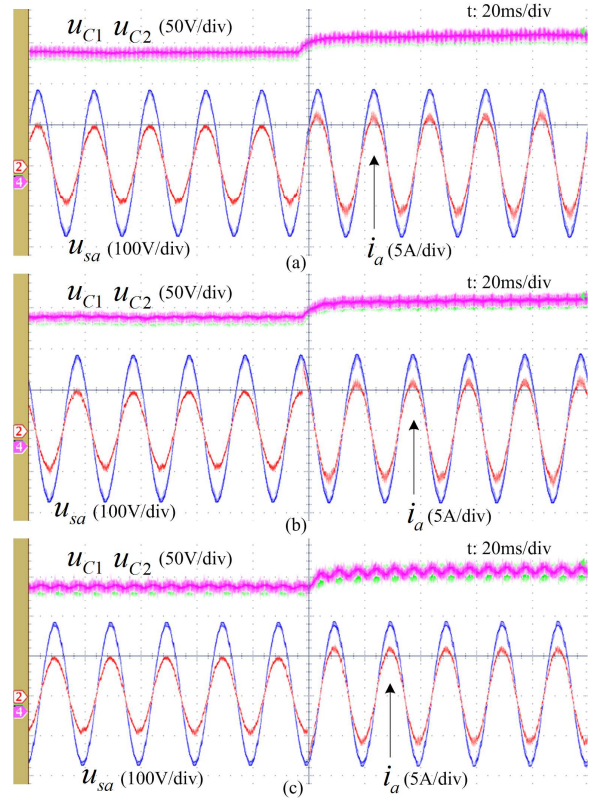


Fig. 15 Experimental results at unity input power factor in (a) approach I; (b) approach II; (c) approach III.

Similarly, Figs. 13(a)-(b) show the related experimental results of approach II; while Figs. 14(a)-(b) show the experimental results of approach III. As seen, the control system with $k = -3$ still come into steady state more rapidly than that with $k = 0$, regardless of which approach it takes. Besides, by comparisons among the results in Figs. 12-14, the capacitor voltages in approach II and III are pulsating with different levels; while they are very smooth in approach I. These results are in line with the theoretic analysis and the related simulation results.

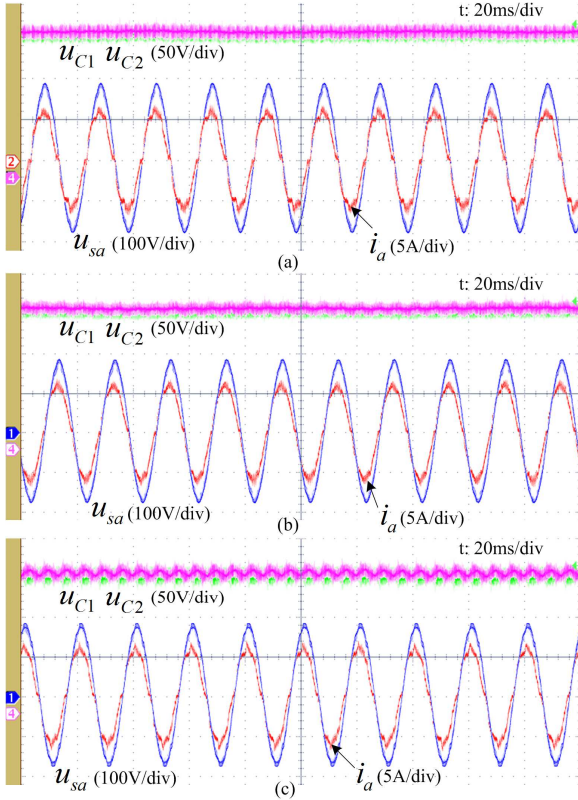


Fig. 16 Experimental results at $\phi_s = \frac{\pi}{18}$ in (a) approach I; (b) approach II; (c) approach III.

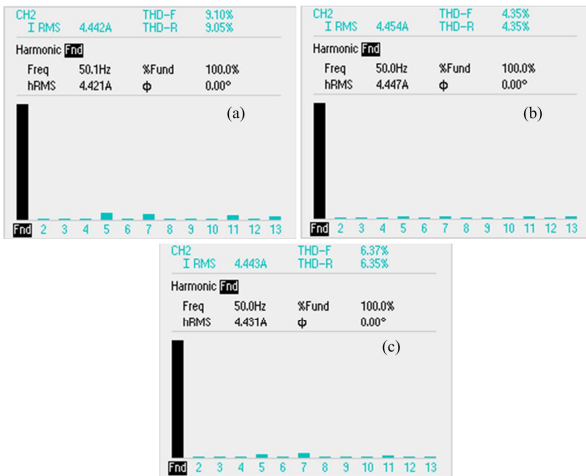


Fig. 17 Spectrum analysis results of input current at $\phi_s = \frac{\pi}{18}$ in (a) approach I (THD=9.1%); (b) approach II (THD=4.35%); (c) approach III (THD=6.37%).

For input current quality analysis, Figs. 15(a)-(c) show the related experimental results of approach I, II and III with unity input power factor, respectively. In such experiments, the desired dc-link voltage changes from 320V to 360V. By comparisons among these results, there are no obvious differences in the current waveforms.

At input power factor angle of $\phi_s = \frac{\pi}{18}$, Figs. 16(a)-(c) show the corresponding experimental results of approach I, II, and III, respectively, with the same conditions in the simulations. As seen, the simulation and experimental waveforms show excellent agreement. Moreover, the spectrum analysis results of the input currents are demonstrated in Figs. 17(a)-(c) successively. From the spectrum graphs, it is found that when the input current distortion is relatively serious, like in Fig. 16(a), low order harmonics, such as 5th and/or 7th harmonics, will exist. Besides, the input current THD is the lowest in approach II, and the highest in approach I, with approach III lying somewhere in between.

In addition, Figs. 18(a)-(b) illustrate the calculated and measured efficiency curves of the three phase Vienna rectifier in the three approaches, respectively. As seen, all the calculated efficiencies are relatively higher than the measured ones, regardless of whichever approach has been used. Further, the (either calculated or measured) efficiency in approach III is always higher than those in the other two approaches due to the reduced switching loss; while they are of little difference approach I and II.

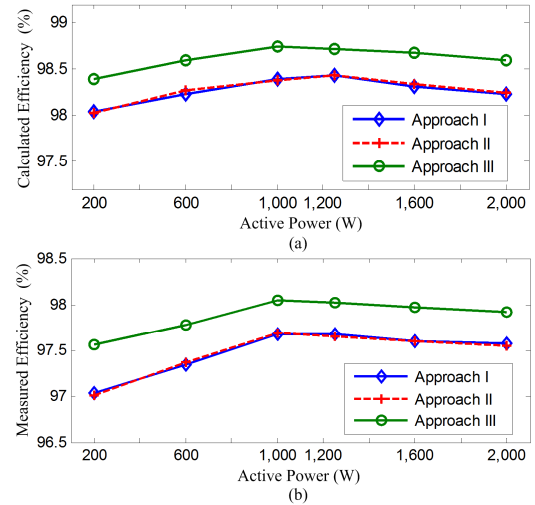


Fig. 18 The curves of the (a) calculated and (b) measured efficiency with regard to active power in the three approaches.

TABLE II
Performance comparisons in three approaches

Approach	Input Current Quality (when $\phi_s = \frac{\pi}{18}$)	Capacitor Voltage Fluctuation	Measured Efficiency (when $P = 1\text{ kW}$)
I	Worse (THD:9.1%)	Small	Slightly lower (97.65%)
II	Better (THD:4.35%)	Middle	Slightly lower (97.62%)
III	Middle (THD:6.37%)	Large	Higher (98.05%)

Generally, the performance comparisons among the three approaches are demonstrated in TABLE II.

VII. CONCLUSION

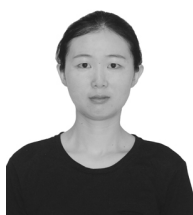
In this paper, a generalized design framework is proposed for the three phase Vienna rectifier to address the issue of neutral point voltage imbalance. Based on the proposed framework, it is convenient to construct different neutral point voltage balance approaches, and the related stability can be guaranteed based on the averaging theory. Through proper construction, neutral point voltage self-balance can be achieved without adding extra feedback control actions. As demonstration, three representative approaches are presented successively, which exhibit different performance characteristics.

Moreover, when the three approaches are used in the Vienna rectifier, the related performances are analyzed and compared in terms of input current quality, capacitor voltage fluctuation, and operating efficiency. Comparatively, approach I can guarantee two capacitor voltages of great coincidence, but the input current quality is the worst of the three at lower power factor. Approach II can obtain the best input current quality, but the steady capacitor voltages have small fluctuations. In approach III, the degree of capacitor voltage fluctuation is even larger than that in approach II, but the operating efficiency is higher than that in the other approaches. In other words, each approach has its own strength and weakness, which can be applied as the related performance is required. Therefore, it can be inferred that new neutral point voltage balance methods can be customized through the proposed design framework according to specific operating performance requirements.

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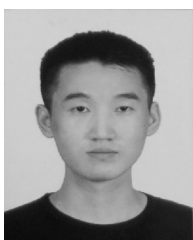
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